

1

2

3

4

5

6

A

B

C

D

E

F

G

H

P1.0	1	40	V _{CC}
P1.1	2	39	P0.0 AD0
P1.2	3	38	P0.1 AD1
P1.3	4	37	P0.2 AD2
P1.4	5	36	P0.3 AD3
P1.5	6	35	P0.4 AD4
P1.6	7	34	P0.5 AD5
P1.7	8	33	P0.6 AD6
RST/VPD	9	32	P0.7 AD7
RXD P3.0	10	31	EA
TXD P3.1	11	30	ALE
INT0 P3.2	12	29	PSEN
INT1 P3.3	13	28	P2.7 A15
TO P3.4	14	27	P2.6 A14
T1 P3.5	15	26	P2.5 A13
WR P3.6	16	25	P2.4 A12
RD P3.7	17	24	P2.3 A11
XTAL2	18	23	P2.2 A10
XTAL1	19	22	P2.1 A9
V _{SS}	20	21	P2.0 A8

STROBE	1	24	V _{DD}
DATA 1	2	23	INHIBIT
DATA 2	3	22	DATA 4
S7	4	21	DATA 3
S6	5	20	S10
S5	6	19	S11
S4	7	18	S8
S3	8	17	S9
S1	9	16	S14
S2	10	15	S15
S0	11	14	S12
V _{SS}	12	13	S13

A7	1	24	V _{CC}
A6	2	23	A8
A5	3	22	A9
A4	4	21	V _{PP}
A3	5	20	CE
A2	6	19	A10
A1	7	18	A11
A0	8	17	O7
O0	9	16	O6
O1	10	15	O5
O2	11	14	O4
GND	12	13	O3

D7	1	24	V _{CC}
D6	2	23	WR
D5	3	22	RD
D4	4	21	CS
D3	5	20	A1
D2	6	19	A0
D1	7	18	CLK 2
D0	8	17	OUT 2
CLK0	9	16	GATE 2
OUT0	10	15	CLK1
GATE0	11	14	GATE 1
GND	12	13	OUT 1

THRESHOLD CONTROL V _{LC}	1	16	COMPENSATION
I _{OUT}	2	15	V _{REF(-)}
V ₋	3	14	V _{REF(+)}
I _{OUT}	4	13	V ₊
MSB B1	5	12	B8 LSB
B2	6	11	B7
B3	7	10	B6
B4	8	9	B5

DISABLE A	1	16	V _{DD}
D1	2	15	DISABLE B
Q1	3	14	D6
D2	4	13	Q6
Q2	5	12	D5
D3	6	11	Q5
Q3	7	10	D4
V _{SS}	8	9	Q4

A7	1	24	V _{CC}
A6	2	23	A8
A5	3	22	A9
A4	4	21	V _{PP}
A3	5	20	OE
A2	6	19	A10
A1	7	18	CE
A0	8	17	O7
O0	9	16	O6
O1	10	15	O5
O2	11	14	O4
GND	12	13	O3

A7	1	24	V _{DD}
A6	2	23	A8
A5	3	22	A9
A4	4	21	RW
A3	5	20	CE ₁
A2	6	19	A10
A1	7	18	CE ₂
A0	8	17	I/O ₈
I/O ₁	9	16	I/O ₇
I/O ₂	10	15	I/O ₆
I/O ₃	11	14	I/O ₅
GND	12	13	I/O ₄

V _{CC} (VCM) (13)	1	14	V _{CC} (OUT BUFFER)
DC CONTROL IN (12)	2	13	
C _x X2 (11)	3	12	
C _x X1 (10)	4	11	
GND (VCM) (9)	5	10	
OUT (8)	6	9	
GND (OUT BUFFER)	7	8	

B4	1	16	V _{DD}
A3	2	15	A4
B3	3	14	Kb
A2	4	13	D4=A4Ka=B4Kb
B2	5	12	D3=A3Ka=B3Kb
A1	6	11	D2=A2Ka=B2Kb
B1	7	10	D1=A1Ka=B1Kb
V _{SS}	8	9	Ka

S	1	16	V _{CC}
I _{0a}	2	15	E
I _{1a}	3	14	I _{0c}
Z _a	4	13	I _{1c}
I _{0b}	5	12	Z _c
I _{1b}	6	11	I _{0d}
Z _b	7	10	I _{1d}
GND	8	9	Z _d

NC	1	8	V _{CC}
ANODE	2	7	V _b
CATHODE	3	6	V ₀
NC	4	5	GND

E _a	1	16	V _{CC}
E _b	2	15	E _b
A ₁	3	14	E _b
O _{3a}	4	13	A ₀
O _{2a}	5	12	O _{3b}
O _{1a}	6	11	O _{2b}
O _{0a}	7	10	O _{1b}
GND	8	9	O _{0b}

PHASE PULSES	1	16	V _{DD}
PHASE COMP. I OUT	2	15	ZENER
COMPARATOR IN	3	14	SIGNAL IN
VCO OUT	4	13	PHASE COMP. II OUT
INHIBIT	5	12	R2 TO V _{SS}
C1	6	11	R1 TO V _{SS}
	7	10	DEMODULATOR OUT
V _{SS}	8	9	VCO IN

MR	1	16	V _{CC}
Q ₀	2	15	Q ₅
D ₀	3	14	D ₅
D ₁	4	13	D ₄
Q ₁	5	12	Q ₄
D ₂	6	11	D ₃
Q ₂	7	10	Q ₃
GND	8	9	CP

E	1	20	V _{CC}
Q ₀	2	19	Q ₇
D ₀	3	18	D ₇
D ₁	4	17	D ₆
Q ₁	5	16	Q ₆
Q ₂	6	15	Q ₅
D ₂	7	14	D ₅
D ₃	8	13	D ₄
Q ₃	9	12	Q ₄
GND	10	11	CP



Denomination:
SCHEMATIC DIAGRAM Mod.
PROJECT 100

Revision:

DWG. 2
8-6-84

1

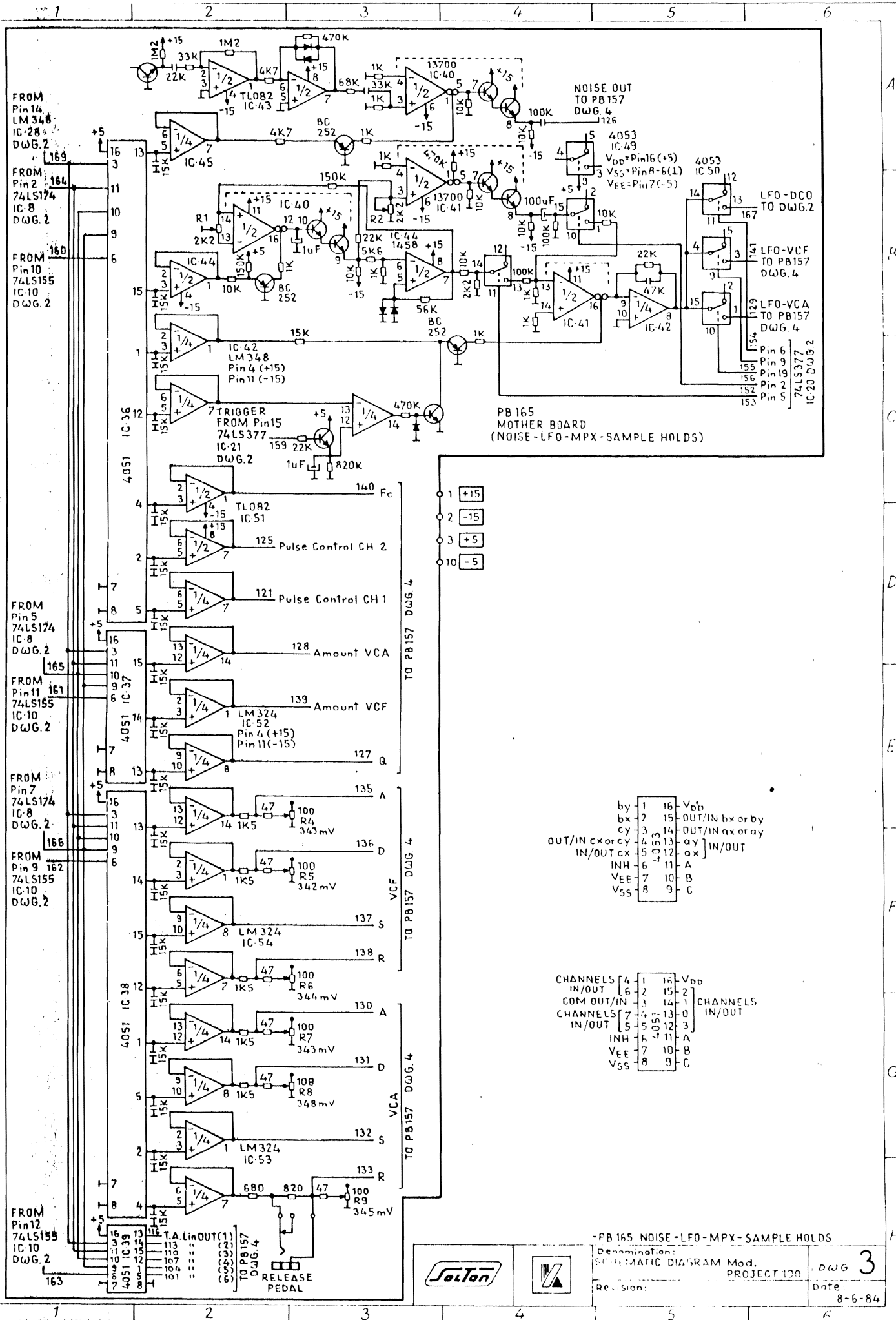
2

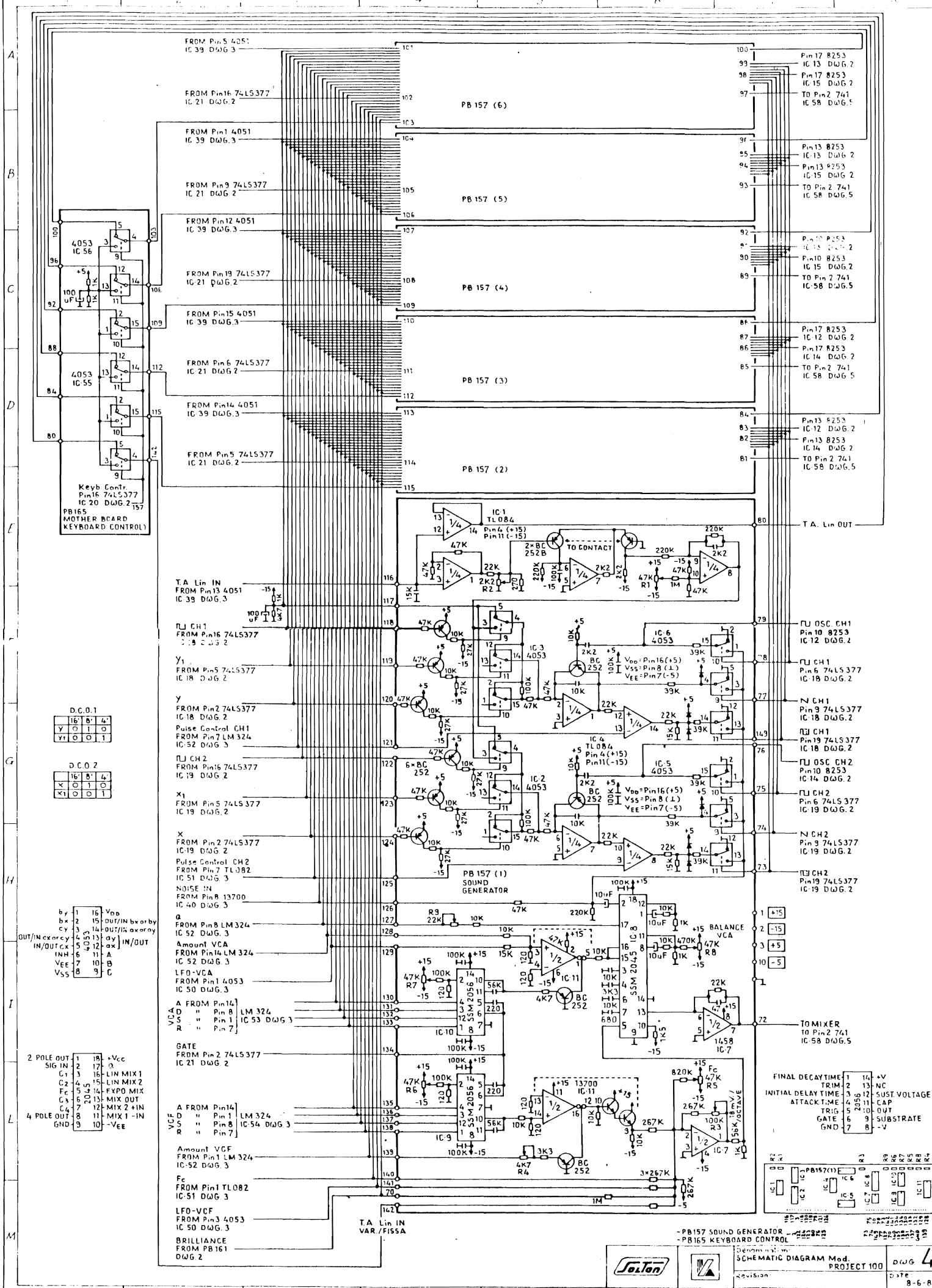
3

4

5

6





Keyb Contr.
Pin16 74LS377
IC 20 DWG.2 157
PB165
MOTHER BOARD
KEYBOARD CONTROL

D.C. 0.1

Y	0	1	0
Y1	0	0	1

D.C. 0.2

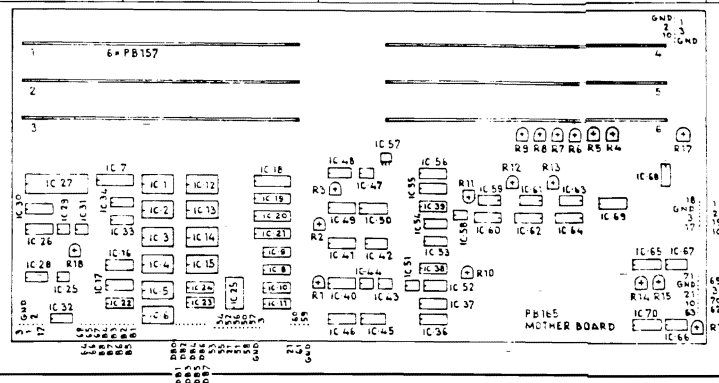
Y	0	1	0
Y1	0	0	1

by 1 16 Vcc
bx 2 15 OUT/IN barby
cy 3 14 OUT/IN away
4 13 ay
5 12 ax IN/OUT
6 11 A
7 10 B
8 9 C
VSS

2 POLE OUT 1 18 +Vcc
SIG IN 2 17 0
C1 3 16 LIN MIX 1
C2 4 15 LIN MIX 2
Fc 5 14 EXPO MIX
C3 6 13 MIX OUT
C4 7 12 MIX 2 +IN
C5 8 11 MIX 1 -IN
4 POLE OUT GND 9 10 -VEE

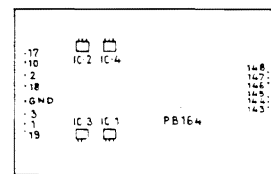
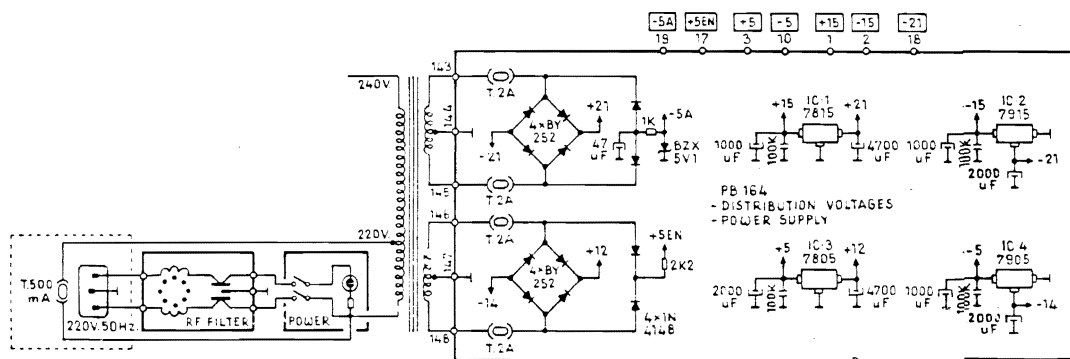
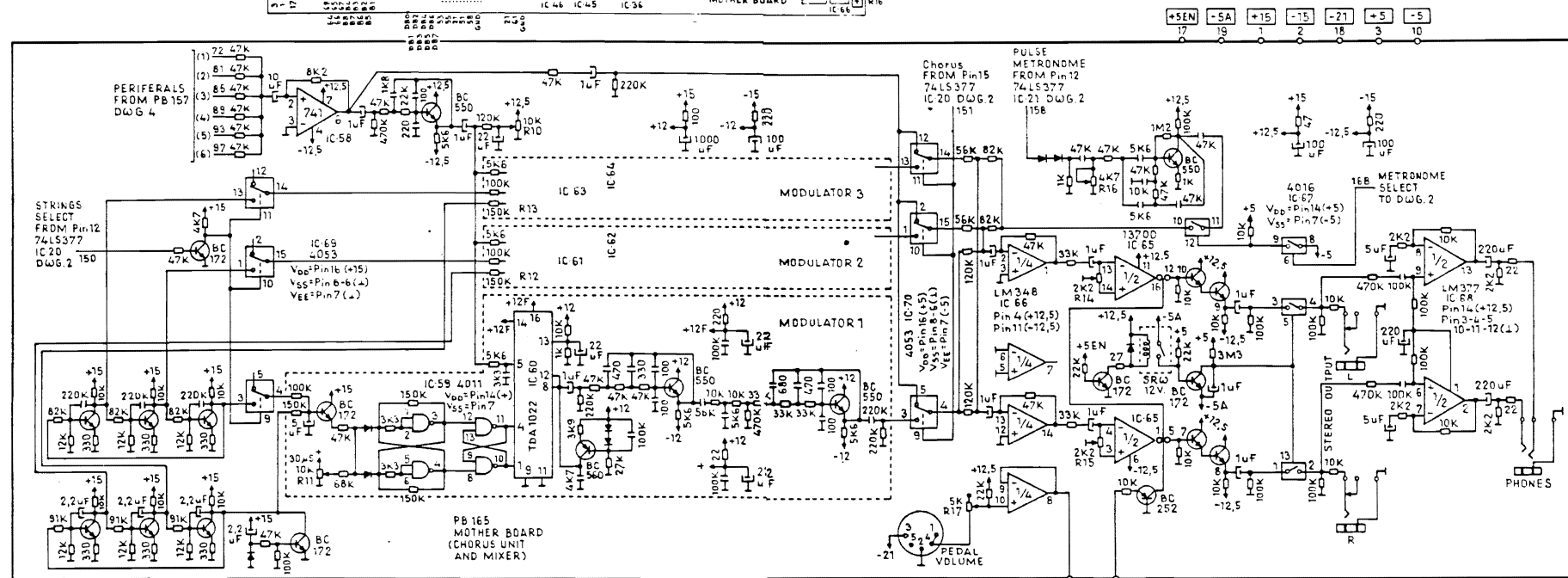
VCF
A FROM Pin14
S " Pin1 LM324
R " Pin7 IC54 DWG.3
Amount VCF
FROM Pin1 LM324
IC52 DWG.3
LFO-VCF
FROM Pin3 4053
IC50 DWG.3
BRILLIANCE
FROM PB161
DWG.2

SIG A IN 1- Vcc
 OUT 2- Control A
 SIG B IN 3- Control B
 OUT 4- IN SIG D
 Control C 5- OUT
 Control D 6- IN SIG C
 Vss 7- IN SIG C



by 1- Vcc
 bx 2- OUT/IN bx or by
 cy 3- OUT/IN bx or by
 OUT/IN cx or cy 4- OUT/IN bx or by
 IN OUT cx 5- OUT/IN bx or by
 IN OUT cy 6- OUT/IN bx or by
 IN OUT dx 7- OUT/IN bx or by
 IN OUT dx 8- OUT/IN bx or by
 VEE 9- VEE
 Vss 10- Vss

Clock Input 1 1- Ground
 NC 2- NC
 NC 3- NC
 Clock Input 2 4- Tetraode gate
 Signal Input 5- Output 512
 NC 6- NC
 NC 7- NC
 Output 513 8- Negative supply



- PB164 POWER SUPPLY
 - PB165 CHORUS UNIT AND MIXER